

tiny SCR PRESELECTOR

I2C Bus control module

The tiny SCR Preselector I2C Bus control module, located in a separate module board, lets to handle easily the Band pass Filter board from an existing control system on your radio project due the simple implementation of the I2C protocol on any microcontroller.

It is based on the well know PCF8575 remote 16-bit I/O expander for I2C Bus. Two power drivers ULN 2803A interface the PCF8575 output ports with the relays. I2C addresses are configured through J4, J5 and J6 pin headers and J2 and J3 headers connect pull-up resistors to the I2C line if is needed.

Three auxiliary ports are provided for optional controls and/or signalling. J7 are Input/Output ports, 5volts/20mA and J8 are buffered output ports at 12volts/500mA level.

J11 provides an open-drain interrupt output which can be connected to the interrupt logic of the microcontroller. Connection to the Multi-band pass filter module is done with 16 ways ribbon cable and IDC connectors on both sides, carrying control signals and power supply.

A carefully PCB design and strong decoupling avoid introduce noise on the filters board.

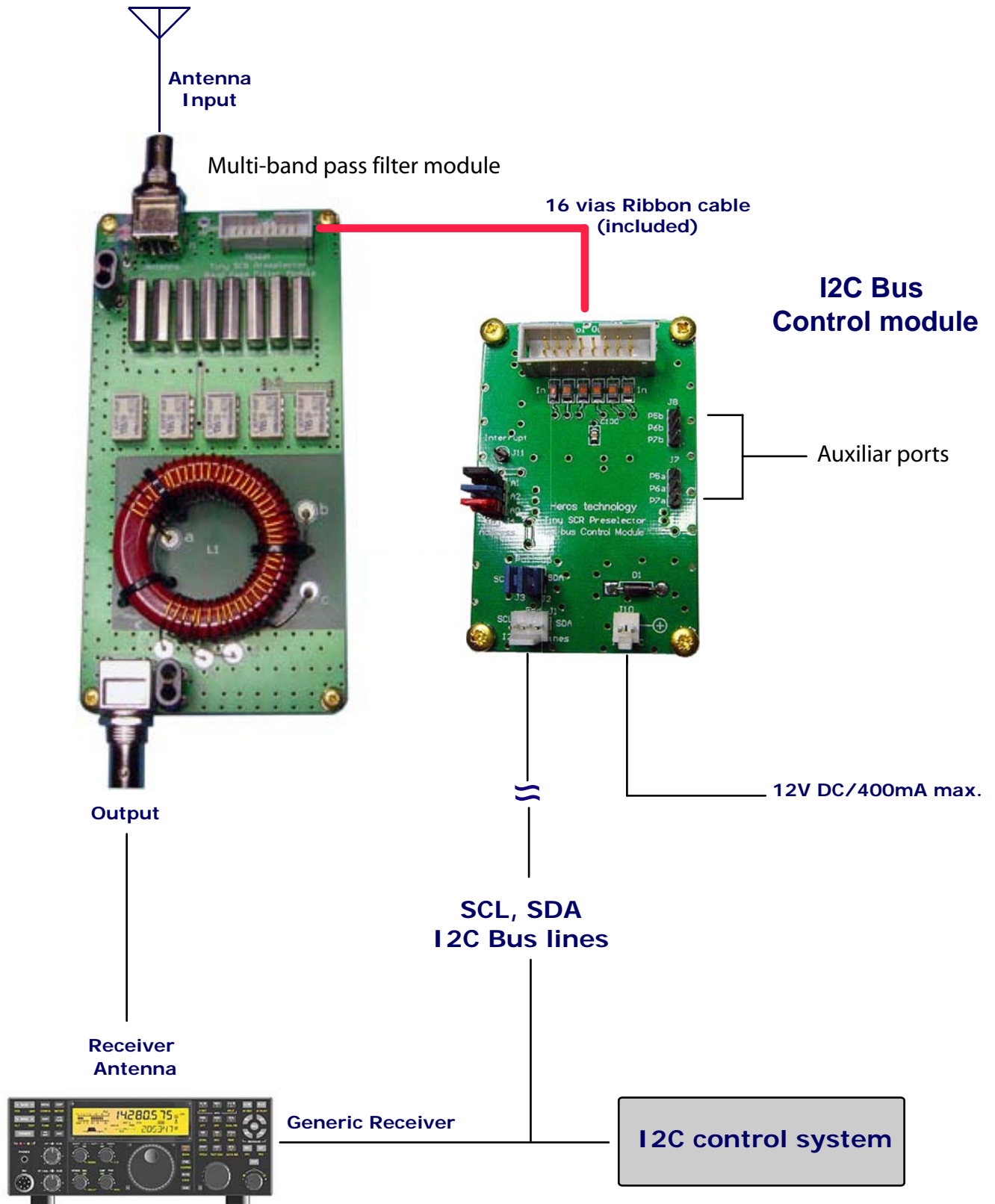
Features of the module are:

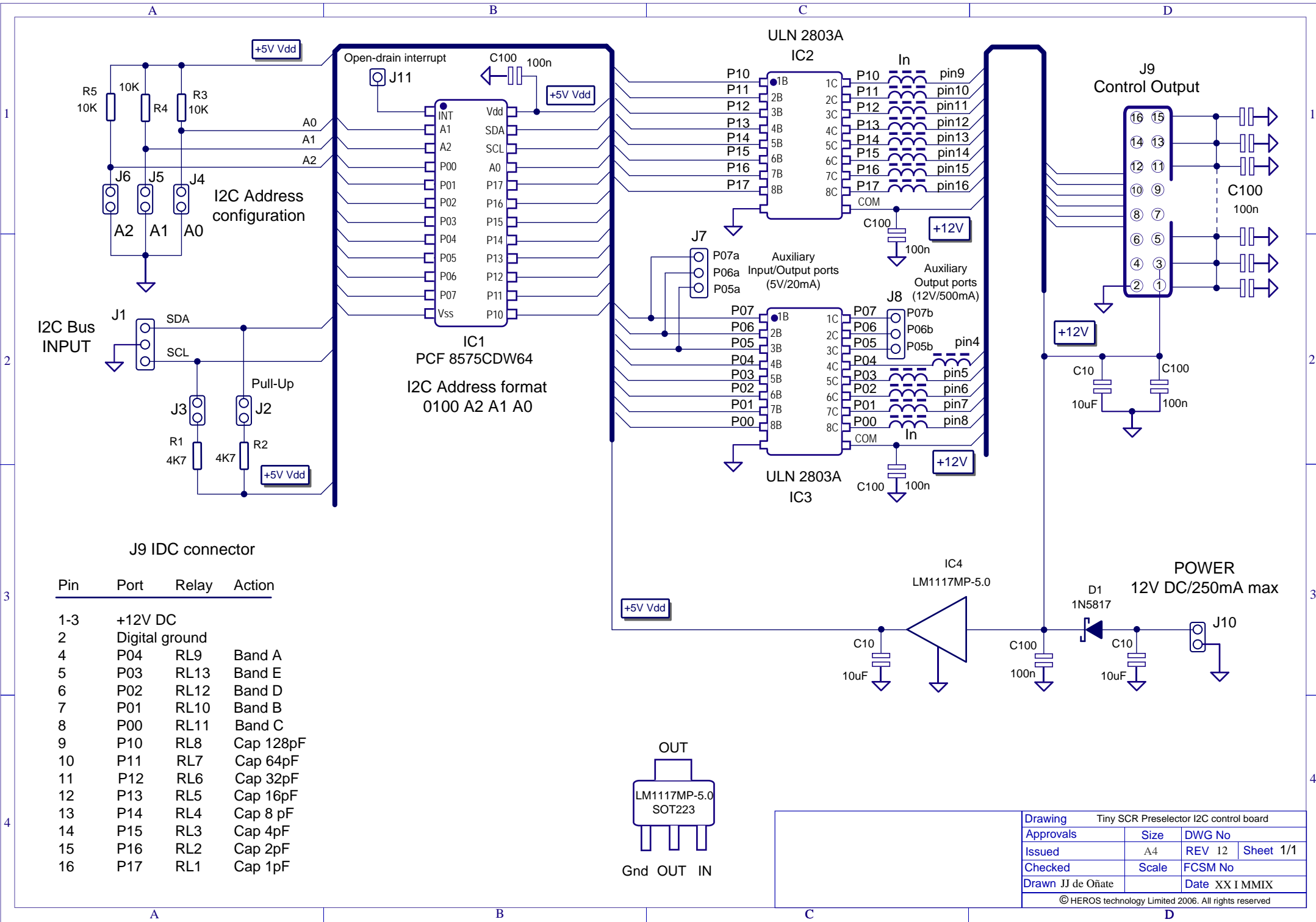
- 16 bits standard I2C serial bus interface.
- 100Kbits/s and 400kbits/s FAST I2C Bus.
- Three auxiliary Input/Output ports for optional controls and/or signalling.
- Open-drain interrupt output.
- Sixteen latched outputs with high current drive capability.
- Programmable address by 3 hardware address pins.
- Optional I2C Bus lines pull-up resistors.
- Up to eight modules can share the same I2C Bus.
- Compatible with most microcontrollers.
- Power Supply: 12V DC/400mA max.
- Dimensions: 62x47mm. (2.44x1.85 inch)

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Tiny SCR Preselector connection



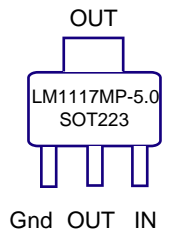


I2C Address configuration

I2C Bus INPUT

J9 IDC connector

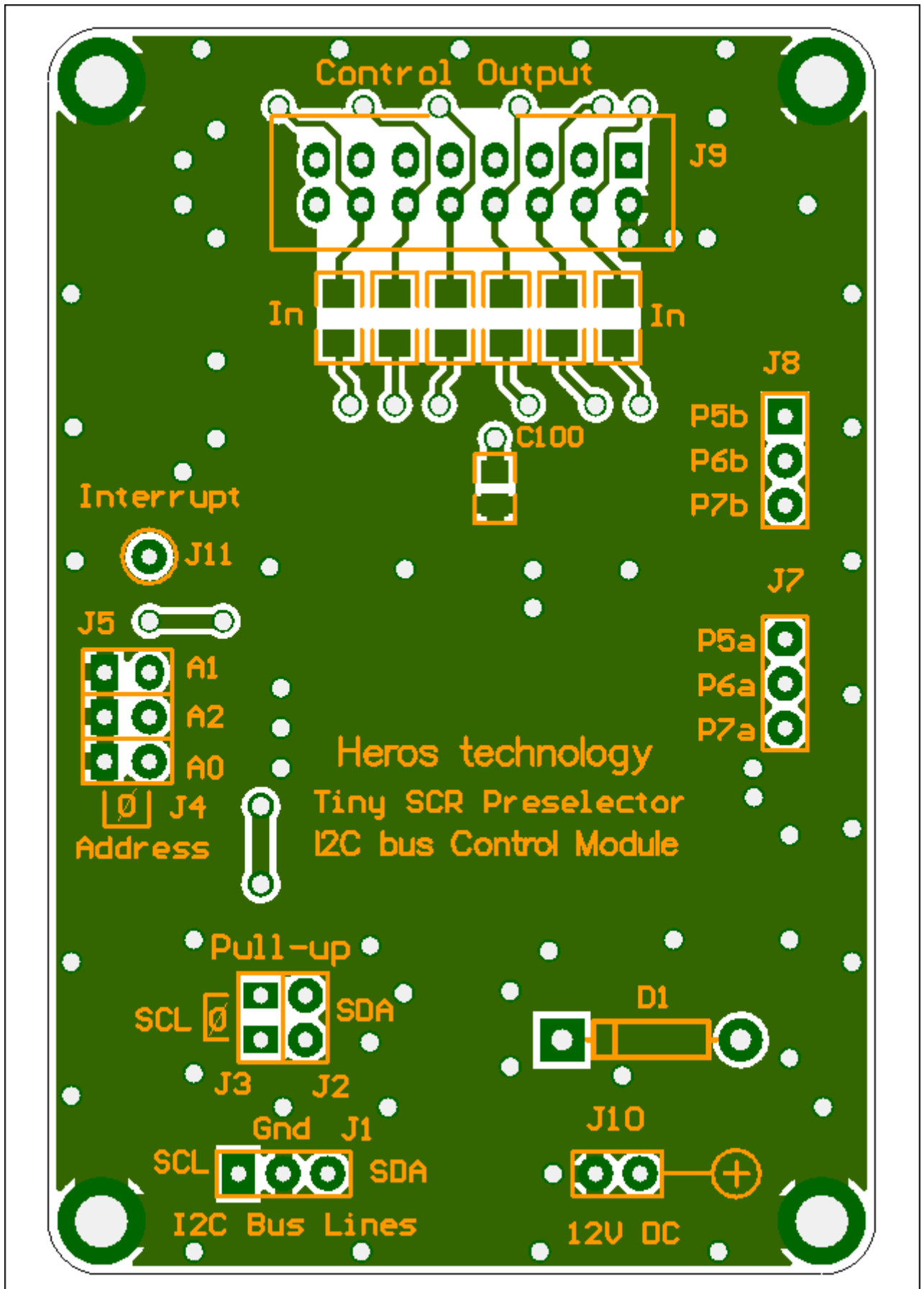
Pin	Port	Relay	Action
1-3	+12V DC		
2	Digital ground		
4	P04	RL9	Band A
5	P03	RL13	Band E
6	P02	RL12	Band D
7	P01	RL10	Band B
8	P00	RL11	Band C
9	P10	RL8	Cap 128pF
10	P11	RL7	Cap 64pF
11	P12	RL6	Cap 32pF
12	P13	RL5	Cap 16pF
13	P14	RL4	Cap 8 pF
14	P15	RL3	Cap 4pF
15	P16	RL2	Cap 2pF
16	P17	RL1	Cap 1pF



Drawing				Tiny SCR Preselector I2C control board			
Approvals		Size	DWG No				
Issued		A4	REV 12	Sheet		1/1	
Checked		Scale	FCSM No				
Drawn JJ de Oñate		Date		XX I MMIX			
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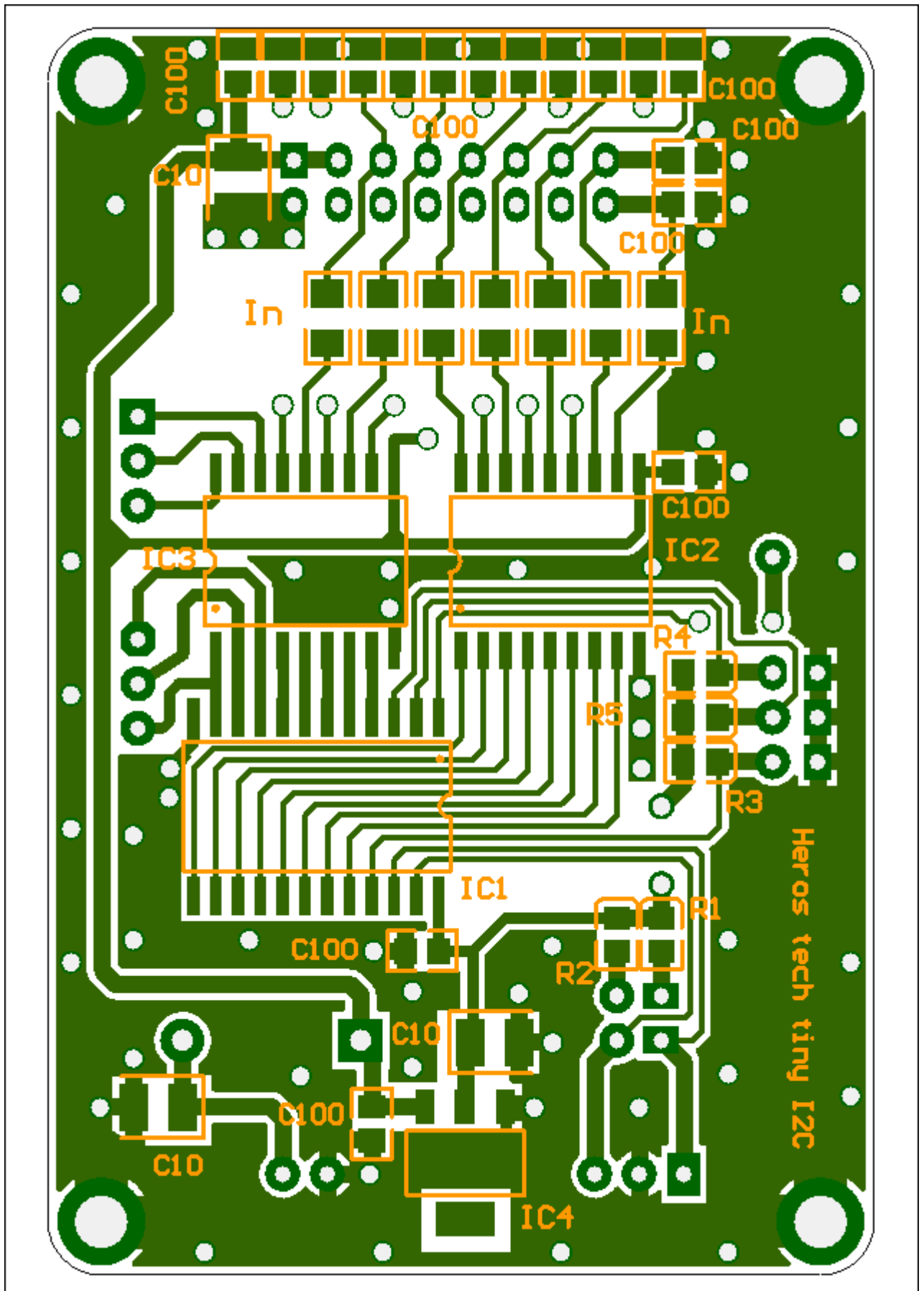
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PCB Bottom

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CHARACTERISTICS OF THE I2C-BUS

The I2C-bus is for bidirectional, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals Fig.1.

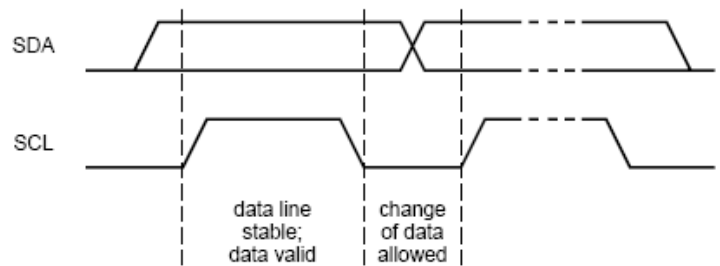


Fig 1

START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition P see Fig.2.

System configuration

A device generating a message is a 'transmitter', a device receiving the message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' see Fig.3.

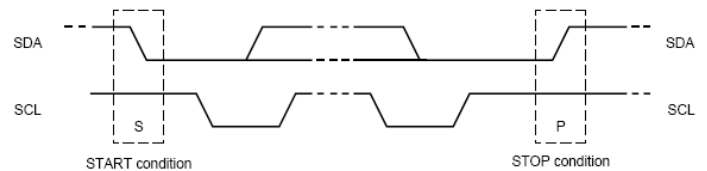


Fig 2

Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The transmitter must release the SDA line before the receiver can send an acknowledge bit. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge after the last byte that has been clocked out of the slave. This is done by the master receiver by holding the SDA line HIGH. In this event the transmitter must release the data line to enable the master to generate a STOP condition. Fig. 4.

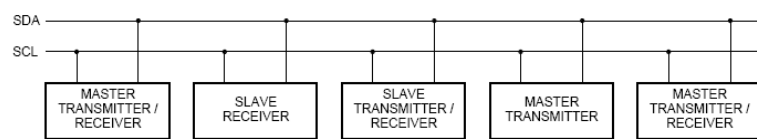


Fig 3

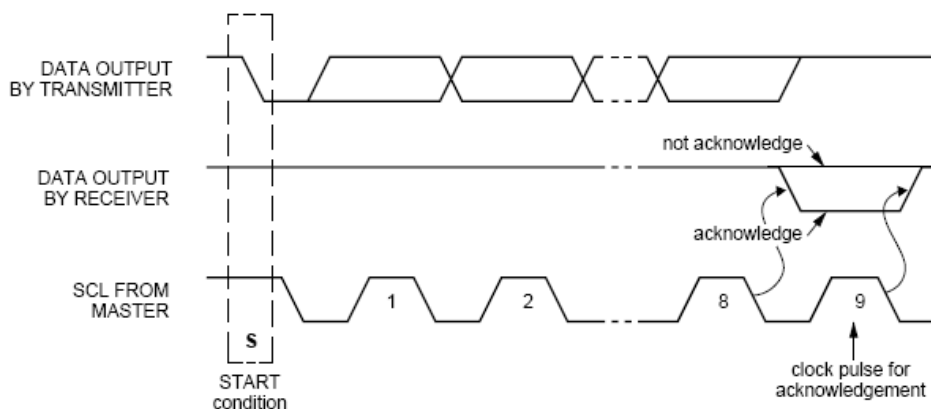


Fig 4

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Quasi-bidirectional I/Os

The PCF8575's 16 ports Fig.5 are entirely independent and can be used either as input or output ports. Input data is transferred from the ports to the microcontroller in the READ mode. Output data is transmitted to the ports in the WRITE mode.

This quasi-bidirectional I/O can be used as an input or output without the use of a control signal for data direction.

At power-on the I/Os are HIGH. In this mode only a current source (I_{OH}) to VDD is active. An additional strong pull-up to VDD (I_{OHt}) allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The I/Os should be HIGH before being used as inputs. After power-on as all the I/Os are set HIGH all of them can be used as input. Any change in setting of the I/Os as either inputs or outputs can be done with the write mode. Warning: If a HIGH is applied to an I/O which has been written earlier to LOW, a large current (I_{OL}) will flow to VSS.

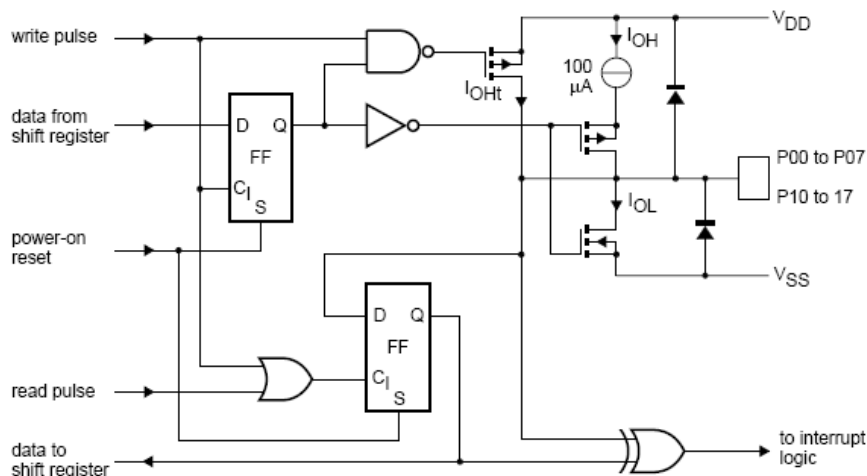


Fig 5

Addressing

Figures 6, 7 and 8 show the address and timing diagrams. Before any data is transmitted or received the master must send the address of the receiver via the SDA line. The first byte transmitted after the START condition carries the address of the slave device and the read/write bit. The address of the slave device must not be changed between the START and the STOP conditions. The PCF8575 acts as a slave receiver or a slave transmitter.

Reading from a port (input mode)

All ports programmed as input should be set to logic 1.

To read, the master (microcontroller) first addresses the slave device after it receives the interrupt. By setting the last bit of the byte containing the slave address to logic 1 the read mode is entered. The data bytes that follow on the SDA are the values on the ports.

If the data on the input port changes faster than the master can read, this data may be lost.

Writing to the port (output mode)

To write, the master (microcontroller) first addresses the slave device. By setting the last bit of the byte containing the slave address to logic 0 the write mode is entered. The PCF8575 acknowledges and the master sends the first data byte for P07 to P00. After the first data byte is acknowledged by the PCF8575, the second data byte P17 to P10 is sent by the master. Once again the PCF8575 acknowledges the receipt of the data after which this 16-bit data is presented on the port lines.

The number of data bytes that can be sent successively is not limited. After every two bytes the previous data is overwritten.

The first data byte in every pair refers to Port 0 (P07 to P00), whereas the second data byte in every pair refers to Port 1 (P17 to P10), see Fig.11.

Interrupt

The PCF8575 provides an open-drain interrupt (INT) which can be fed to a corresponding input of the microcontroller. This gives these chips a kind of a master function which can initiate an action elsewhere in the system. An interrupt is generated by any rising or falling edge of the port inputs. After time t_{iv} the signal INT is valid.

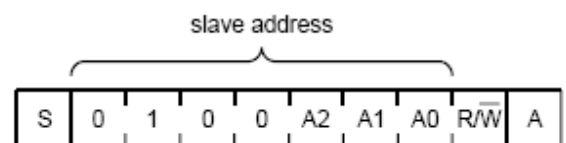


Fig 6

Byte containing the slave address and the R/W bits.

The interrupt disappears when data on the port is changed to the original setting or data is read from or written to the device which has generated the interrupt.

In the write mode the interrupt may become deactivated (HIGH) on the rising edge of the write to port pulse. On the falling edge of the write to port pulse the interrupt is definitely deactivated (HIGH).

The interrupt is reset in the read mode on the rising edge of the read from port pulse.

During the resetting of the interrupt itself any changes on the I/Os may not generate an interrupt. After the interrupt is reset any change in I/Os will be detected and transmitted as an INT.

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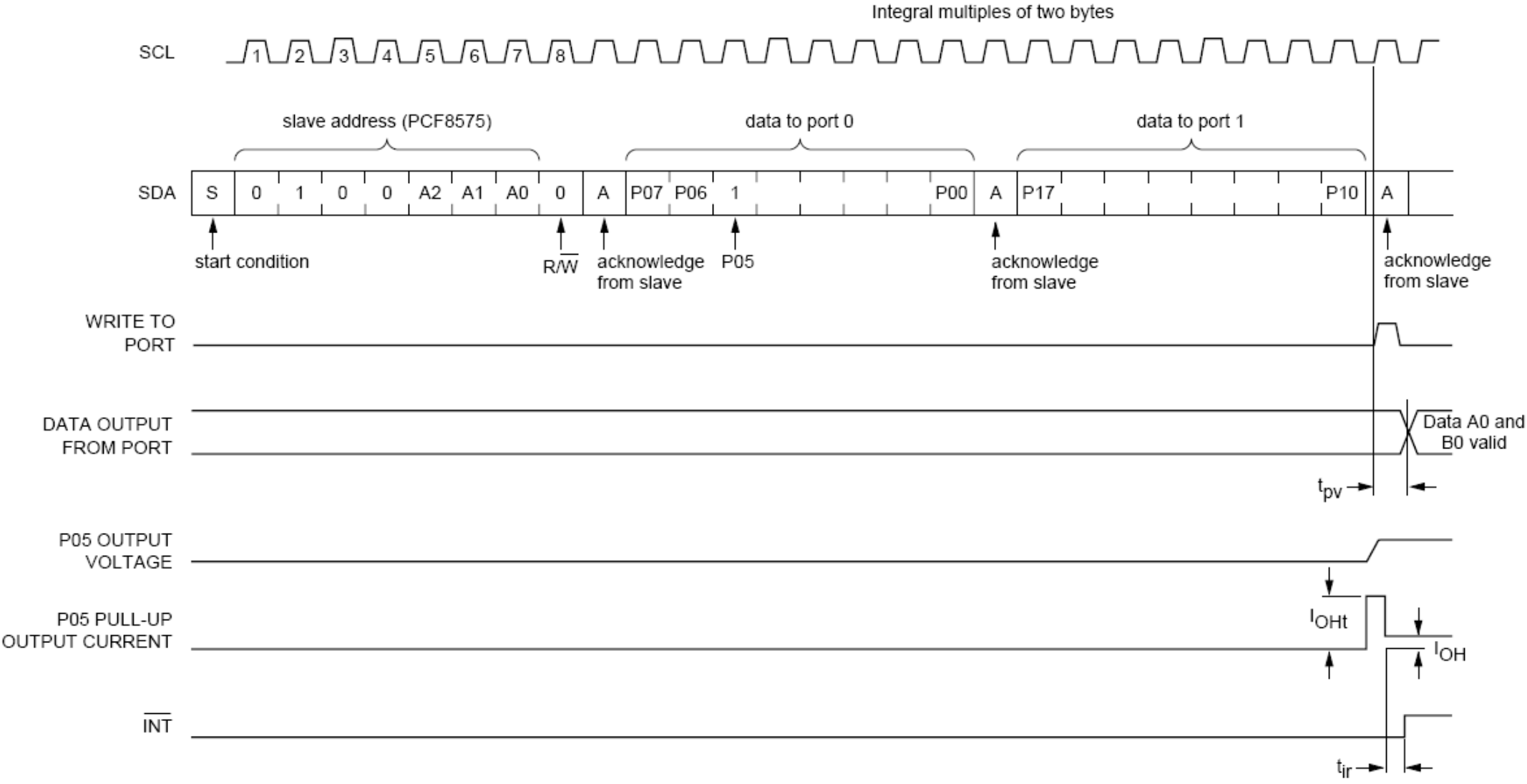
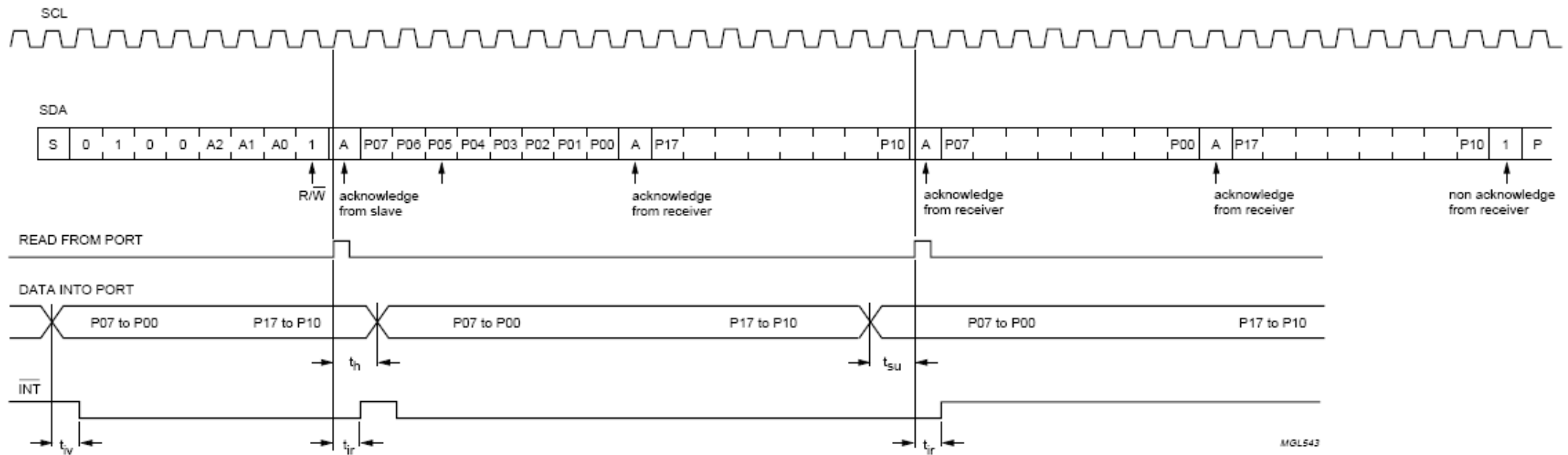


Fig.7 Write mode (output).

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A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the STOP condition (P). Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). Input data is lost.

Fig.8 READ mode (input).

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Reading from a port (input mode)

All ports programmed as input should be set to logic 1. To read, the master (microcontroller) first addresses the slave device after it receives the interrupt. By setting the last bit of the byte containing the slave address to logic 1 the read mode is entered. The data bytes that follow on the SDA are the values on the ports. If the data on the input port changes faster than the master can read, this data may be lost.

Writing to the port (output mode)

To write, the master (microcontroller) first addresses the slave device. By setting the last bit of the byte containing the slave address to logic 0 the write mode is entered. The PCF8575 acknowledges and the master sends the first data byte for P07 to P00. After the first data byte is acknowledged by the PCF8575, the second data byte P17 to P10 is sent by the master. Once again the PCF8575 acknowledges the receipt of the data after which this 16-bit data is presented on the port lines. The number of data bytes that can be sent successively is not limited. After every two bytes the previous data is overwritten. The first data byte in every pair refers to Port 0 (P07 to P00), whereas the second data byte in every pair refers to Port 1 (P17 to P10), Fig.9.

Interrupt

The PCF8575 provides an open-drain interrupt (INT) which can be fed to a corresponding input of the microcontroller. This gives these chips a kind of a master function which can initiate an action elsewhere in the system. An interrupt is generated by any rising or falling edge of the port inputs. After time t_{iv} the signal INT is valid. The interrupt disappears when data on the port is changed to the original setting or data is read from or written to the device which has generated the interrupt. In the write mode the interrupt may become deactivated (HIGH) on the rising edge of the write to port pulse. On the falling edge of the write to port pulse the interrupt is definitely deactivated (HIGH). The interrupt is reset in the read mode on the rising edge of the read from port pulse. During the resetting of the interrupt itself any changes on the I/Os may not generate an interrupt. After the interrupt is reset any change in I/Os will be detected and transmitted as an INT.

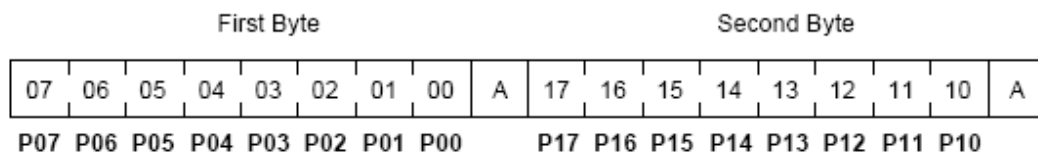


Fig.9 Correlation between bits and ports.

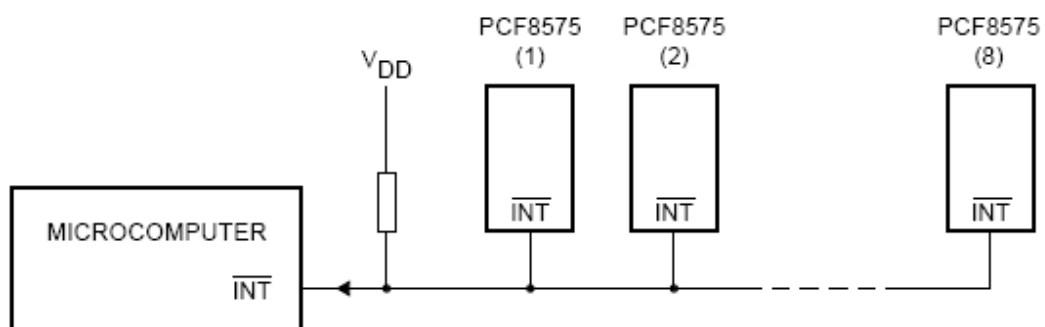
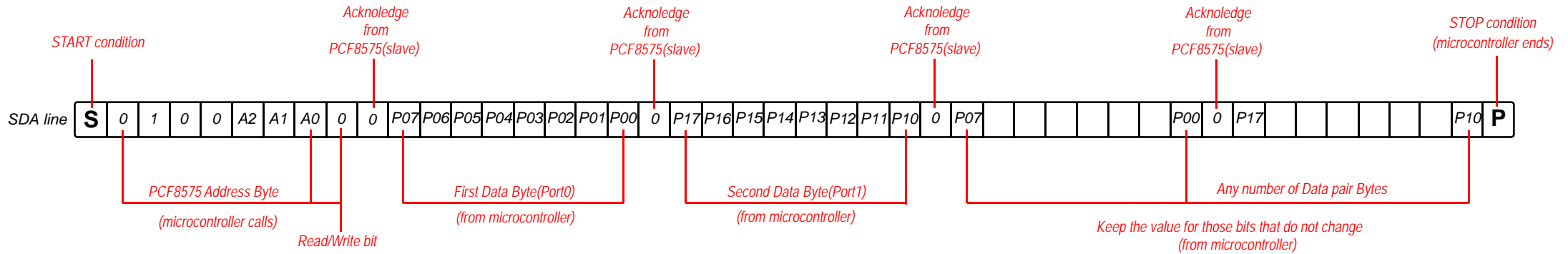
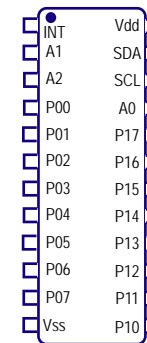


Fig.10 Application of multiple PCF8575s with interrupt.

Write sequence (8 bits Bytes) (microcontroller transmits data to PCF8575)



Port	Relay	Action
P00	RL11	Band C
P01	RL10	Band B
P02	RL12	Band D
P03	RL13	Band E
P04	RL9	Band A
P05		Auxiliar Input/Output
P06		Auxiliar Input/Output
P07		Auxiliar Input/Output
P10	RL8	Cap 128pF
P11	RL7	Cap 64pF
P12	RL6	Cap 32pF
P13	RL5	Cap 16pF
P14	RL4	Cap 8 pF
P15	RL3	Cap 4pF
P16	RL2	Cap 2pF
P17	RL1	Cap 1pF



PCF 8575DW
I2C Address format
0100 A2 A1 A0

**A0,A1,A2 address bits
set by hardware**

NOTES:

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